ENGLISH TRANSLATION OF INTERNATIONAL APPLICATION AS ORIGINALLY FILED

DESCRIPTION

PROCESS FOR PRODUCING COMPONENT-EMBEDDED SUBSTRATE

Technical Field

The present invention relates to a process for producing a substrate containing an electronic component, such as a semiconductor element and a chip component, therein.

Background Art

Demands for miniaturization and higher performance of electronic devices require a further reduction in profile of components each having a smaller mounting area. To meet such requirements, a component-embedded substrate in which multiple resin layers each including a semiconductor element and a chip component therein are laminated is known.

Patent Document 1 (Japanese Unexamined Patent Application Publication No. 2002-76637) proposes a process for producing the component-embedded substrate by press-bonding and transferring a supporting layer including a component-connected electrode pattern onto one surface of a prepreg, and then laminating the resulting prepreg with another prepreg in which a component is embedded by press bonding in a single step.

Fig. 8 is an example shown in Fig. 15 in Patent Document 1. In step (a), a prepreg 1501 including via holes 1502 and a supporting layer 1504 including an electrode pattern on which electronic components 1510 and 1511 are connected are prepared.

In step (b), these are laminated by press bonding. In step (c), the supporting layer 1504 is separated to form a wiring layer 1515. In step (d), the wiring layer 1515, another wiring layer 1514 in which an electronic component 1505 is embedded, wiring layers 1512 and 1513 including an electrode pattern 1506 and an interlayer via 1507, respectively, are laminated by press bonding in a single step to form a multilayer component-embedded substrate 1516 as shown in (e).

However, in such a single-step lamination process, at the interlayer between the laminated prepregs, an electrode pattern transferred on the surfaces of the prepregs is only in contact with another electrode pattern or an electronic component to provide an electrical connection, thus disadvantageously increasing connection resistance and resulting in insufficient connection reliability. Furthermore, since two electrode layers are disposed between the laminated prepregs, the bonding strength between the prepregs is low, thus possibly causing delamination.

To overcome the problems, in Fig. 16 in Patent Document 1, a process in which a prepreg to be an adhesive layer including a through hole is provided between the cured resin layers to ensure the connection reliability between the electrode patterns or between the electrode pattern and the electronic component is also proposed. However, this process disadvantageously requires the interlayer prepreg having no component, thus increasing the thickness of the component-embedded substrate.

Accordingly, it is an object of the present invention to

provide a process for producing a component-embedded substrate having low connection resistance between laminated electrode patterns or between an electrode pattern and an electronic component, the electrode pattern and the electronic component being laminated, and having improved connection reliability.

It is another object of the present invention to provide, when electronic components are connected onto front and back surfaces of an inner layer electrode, a process for producing a component-embedded substrate having improved connection reliability between the inner layer electrode and the electronic components

Disclosure of Invention

To achieve the objects, according to a first embodiment of the present invention, there is provided a process for producing a component-embedded substrate, including the steps of connecting and fixing a first electronic component to a first electrode pattern on a first supporting layer with a conductive bonding material; press-bonding a second supporting layer including a second electrode pattern onto the electronic component-fixed surface of the first supporting layer with a first prepreg therebetween to perform transfer; separating the first supporting layer and the second supporting layer from the first prepreg; curing the first prepreg before or after the separating step; connecting and fixing a second electronic component onto the back surface of the second electrode pattern with a conductive bonding material; press-bonding a third supporting layer including a third electrode pattern onto a second electronic component-fixed surface with a second prepreg therebetween to perform transfer; separating the third supporting layer from the second prepreg; and curing the

second prepreg before or after the separating step, wherein the prepregs and the electrode patterns are sequentially laminated through the steps.

According to a second embodiment of the present invention, there is provided a process for producing a component-embedded substrate including the steps of connecting and fixing a first electronic component on the surface of an electrode pattern on a supporting layer with a conductive bonding material; press-bonding a first prepreg onto the first electronic component-fixed surface of the supporting layer; separating the supporting layer from the first prepreg; curing the first prepreg before or after the separating step; connecting and fixing a second electronic component onto the back surface of the electrode pattern with a conductive bonding material; press-bonding a second prepreg onto the second electronic component-fixed surface; and curing the second prepreg.

According to a third embodiment of the present invention, there is provided a process for producing a component-embedded substrate including the steps of connecting and fixing a first electronic component onto the surface of a first electrode pattern on a first supporting layer with a conductive bonding material; press-bonding a second supporting layer including a second electrode pattern onto the electronic component-fixed surface of the first supporting layer with a first prepreg therebetween to perform transfer; separating the first supporting layer and the second supporting layer from the first prepreg; curing the first prepreg before or after the separating step; connecting and fixing

a second electronic component onto the back surface of the first electrode pattern with a conductive bonding material; press-bonding a third supporting layer including a third electrode pattern onto a second electronic component-fixed surface with a second prepreg therebetween to perform transfer; separating the third supporting layer from the second prepreg; and curing the second prepreg before or after the separating step, wherein the prepregs and the electrode patterns are sequentially laminated through the steps.

According to the first embodiment of the present invention, a plurality of layers are not laminated in a single step but sequentially laminated. The first electronic component is connected and fixed onto the first electrode pattern with the conductive bonding material. The first electrode pattern is integrally press-bonded to the second electrode pattern with the first prepreg therebetween. In this case, a process for transferring the electrode patterns by forming the electrode patterns on the supporting layers, press-bonding the resulting electrode patterns to the prepregs, and then performing separation is employed. Next, the second electronic component is connected and fixed onto the back surface of the second electrode pattern with the conductive bonding material. The third electrode pattern is press-bonded and transferred onto the resulting second electrode pattern with the second prepreg therebetween.

In this way, by sequentially laminating the prepregs and the electrode patterns, it is possible to produce a component-embedded substrate having a multilayer structure.

The electrode pattern is connected to the electronic component

with the conductive bonding material (solder, a conductive adhesive, a bump, or the like), thus reducing connection resistance between the electrode pattern and the electronic component and achieving high connection reliability.

According to the first embodiment, the electrode pattern is transferred to the prepreg. After curing this prepreg, the next prepreg is press-bonded simultaneously with the transfer of the electrode pattern to the surface. Consequently, the resulting inner layer electrode between the prepregs (resin layers) is a single layer alone and is different from the conventional structure having two inner layer electrodes. Therefore, it is unnecessary to contact and electrically connect the inner layer electrodes to each other. Furthermore, it is possible to prevent the occurrence of delamination between the inner layer electrodes.

The electrode pattern is transferred to the prepreg, and after curing this prepreg, the next prepreg is laminated; hence, the first prepreg is not compressed every lamination, and there is no problem, such as the poor electrical connection of the electrical component embedded in the first prepreg or the deformation of the electrode pattern.

Curing of the prepreg may be performed before or after separation of the supporting layer.

According to the second embodiment of the present invention, when the electronic components are connected onto the front and back surfaces of the inner layer electrode, there is provided the process in which the electronic component is connected and fixed onto the surface of the electrode pattern with the conductive bonding material, this is transferred to the first prepreg, the

first prepreg is cured, the second electronic component is connected and fixed onto the back surface of the electrode pattern with the conductive bonding material, and the second prepreg is press-bonded thereon.

Conventionally, in the case of in which electronic components are connected onto the front and back surfaces of an inner layer electrode, the electrodes of the electronic components must be brought into contact with and electrically connected to the inner layer electrode, thus disadvantageously resulting in low conduction reliability and high connection resistance between the component electrodes and the inner layer electrode. In contrast, according to the second embodiment, not only a process in which lamination is sequentially performed one layer at a time is employed but also the second electronic component is connected and fixed onto the back surface of the first electrode pattern with the conducive bonding material, the first electrode pattern connecting and fixing the first electronic component on the front surface with the conducive bonding material, thus resulting in high conduction reliability and low connection resistance between the inner layer electrode and the electronic component.

Also in this case, after curing the first prepreg, the second prepreg is press-bonded as in the case according to the first embodiment. Thus, it is possible to prevent the deviation and the breakage of the electrode pattern transferred to the first prepreg, a poor connection between the electronic component and the electrode pattern, and the like. Furthermore, the delamination between the prepregs does not occur.

According to the third embodiment, in the step of press-

bonding the first prepreg and the second prepreg in the process according to the second embodiment, a substep of disposing the supporting layer having the electrode pattern on the surface opposite the press-bonded surface of the prepreg and then press-bonding this supporting layer to the prepreg simultaneously with the above-described press-bonding step is included, and after the press-bonding substep, the second supporting layer is separated from the prepreg to transfer the electrode pattern to the prepreg.

In the process according to the second embodiment, when the electrode pattern is provided on the surface opposite the press-bonded surface of the prepreg, there is a process of separately forming a thick-film electrode pattern or a thin-film electrode pattern after curing the prepreg. This disadvantageously increases the number of steps.

Accordingly, in the process according to the third embodiment, by simultaneously transferring the electrode patterns to both front and back surfaces, it is unnecessary to form new electrode pattern after press-bonding the prepreg. Therefore, the number of steps can be reduced.

According to a fourth embodiment, the process preferably further includes the steps of forming a through hole in the resin layer across the thickness direction after curing the prepreg; and forming a conducting path inside the hole, the conducting path electrically connecting the electrode patterns provided on the front surface and the back surface of the resin layer.

Conventionally (in Patent Document 1), a through hole is formed in a prepreg and is then filled with a conducting material. After performing lamination, the prepreg is thermally cured.

However, during the thermal curing, the contraction of the prepreg due to curing may cause the deviation of the position of the electrode pattern being in contact with the through hole, thus possibly reducing connection reliability.

In contrast, in accordance with the fourth embodiment, after curing the prepreg, a hole (a through hole or a via hole) is provided, and a conducting path is formed inside the hole. Therefore, it is possible to surely connect the hole with the electrode patterns without the positional deviation of the electrode patterns on the front and back surfaces of the resin layer.

As a process for forming the conducting path, the inner surface of the hole may be subjected to plating. Alternatively, the conducting path may be formed by filling the inside of the hole with a conducting paste and then curing the paste.

According to a fifth embodiment, the process may further include the steps of forming the hole connecting the electrode pattern provided on the front surface or the back surface of the resin layer with the external electrode of the electronic component after curing the prepreg; and forming the conducting path inside the hole, the conducting path electrically connecting the electrode pattern with the external electrode of the electronic component.

In accordance with the fourth embodiment, the electrode patterns on the front and back surfaces of the resin layer are connected to each other. On the other hand, in accordance with the fifth embodiment, one of the electrode patterns is directly connected to the external electrode of the electronic component. The wiring resistance of the through holes and via holes is higher

than that of usual copper wiring. Therefore, the hole desirably has the minimum length. In this case, since the length of the hole can be reduced by the thickness of the component, the resistance of the conducting path can be advantageously reduced.

In accordance with a sixth embodiment, the step of curing the prepreg may include a substep of performing temporary curing before separating the supporting layer from the prepreg; and performing complete curing after separating the supporting layer from the prepreg.

When the supporting layer is separated without curing the prepreg, the problems, such as the difficulty of the separation of the supporting layer or the breakage of the prepreg, may occur because of the adhesion between the prepreg and the supporting layer. In contrast, performing temporary curing before separating the supporting layer from the prepreg permits easy separation of the supporting layer from the prepreg while the deformation of the prepreg is prevented.

When the next prepreg is laminated in the temporarily cured state, the prepreg being in the temporarily cured state may be deformed by compression. Therefore, complete curing should be performed before the lamination of the next prepreg.

When an epoxy resin is used in the prepreg, as the temporary curing conditions, for example, heat treatment should be performed at 120°C for about 10 to 15 minutes. As the complete curing conditions, heat treatment should be performed at 170°C to 200°C for about 1 hour.

In accordance with a seventh embodiment, after curing the

second prepreg, a step of press-bonding a fourth supporting layer having a fourth electrode pattern onto the surface of the first prepreg with a third prepreg therebetween to perform transfer, the surface being opposite the surface bonded to the second prepreg; a step of separating the fourth supporting layer from the third prepreg; and curing the prepreg before or after the separating step, may be provided.

When three or more prepregs are laminated, a process of laminating a second prepreg serving as a second layer on a first prepreg serving as a first layer and then laminating a third prepreg serving as a third layer on the second layer prepreg is conceivable. However, the first resin layer (prepreg) is warped toward the second layer prepreg by the contraction of the second layer prepreg due to curing. Thus, when the third layer prepreg is laminated thereon, the resulting laminate is further warped by the contraction of the third layer prepreg due to curing.

Accordingly, in the seventh embodiment, when the second layer prepreg is laminated on the first layer prepreg, the third layer prepreg is laminated not on the second layer prepreg but on the first layer prepreg. As a result, the influence of the warpage caused by the contraction of the second layer prepreg due to curing is compensated with the contraction of the third layer prepreg due to curing, thereby resulting in a laminate with a low warpage as a whole.

Brief Description of the Drawings

Fig. 1 is a cross-sectional view of a component-embedded substrate produced by a production process according to a first embodiment of the present invention,

Fig. 2 is a process chart for producing the component-embedded substrate shown in Fig. 1.

Fig. 3 is a process chart for producing the component-embedded substrate according to a second embodiment of the present invention.

Fig. 4 is a process chart for producing the component-embedded substrate according to a third embodiment of the present invention.

Fig. 5 is a process chart for producing the component-embedded substrate according to a fourth embodiment of the present invention.

Fig. 6 is a perspective view of a component-embedded substrate according to a fifth embodiment of the present invention.

Fig. 7 is a process chart for producing the component-embedded substrate according to a sixth embodiment of the present invention.

Fig. 8 is a process chart for producing a conventional component-embedded substrate.

Best Mode for Carrying Out the Invention

Fig. 1 shows a component-embedded substrate A produced by a process according to a first embodiment of the present invention.

In the figure, reference numerals 1 and 2 represent resin layers constituting the substrate. Patterned outer layer electrodes 3 and 4 are provided on the front and back surfaces of the resin layers 1 and 2, respectively. A patterned inner layer electrode 5 is provided between the resin layers 1 and 2. An electronic component 6 is connected and fixed onto the inner surface of the outer layer electrode 4, which is provided the lower side, with a conductive bonding material 7. An electronic component 8 is connected and fixed onto the upper surface of the

inner layer electrode 5 with a conductive bonding material 9. As the conductive bonding materials 7 and 9, solder, conducting adhesives, bumps, or the like are used. The outer layer electrode 4, which is provided the lower side, is appropriately connected to the inner layer electrode 5 through a via hole 10 filled with a conducting material. The outer layer electrode 3, which is provided the upper side, is appropriately connected to the inner layer electrode 5 through a via hole 11.

The via holes 10 and 11 each have a diameter of, for example, 100 to 500 μm and a length of 100 to 1,000 μm, and are formed by a laser or drilling. As a conducting material with which the via holes 10 and 11 are filled, for example, a binder that is composed of glass, a resin, or the like and that contains Cu, Ag, Ni, Au, Sn, Zn, Pd, or Pt or a mixture of these serving as a conductive material is preferably used, the content of the conductive material being 20% to 90%.

The outer layer electrodes 3 and 4 and the inner layer electrode 5 are each formed of, for example, a metal thin film having a thickness of 10 to 40 μm. As the electrodes 3, 4, and 5, for example, a copper foil is used. The copper foil may be subjected to gold plating, tin plating, or preflux treatment.

As the resin layers 1 and 2, for example, an epoxy resin containing an inorganic filler is used. The content of the inorganic filler is, for example, 60% to 95%. The inorganic filler is composed of an insulating material, such as SiC, Al_2O_3, or AlN, and preferably has a size of, for example, 0.1 to 10 μm. In this way, by incorporating the inorganic filler, the linear expansion coefficient of the prepreg described below can be

reduced and thus can be brought close to the linear expansion coefficient of a wiring material constituting the electrode pattern and to the linear expansion coefficient of the conductive bonding material. Furthermore, stress applied to a junction during heating can be reduced. Therefore, the reliability of the junction can be improved.

A process for producing the component-embedded substrate A having a structure described above will be described below according to Fig. 2. This production process corresponds to the first embodiment.

In step (a), an electrode that is formed of a copper foil or the like and that is bonded onto a supporting layer 12 is etched to form a circuit pattern 4. The circuit pattern 4 may be directly formed on the supporting layer 12 by plating, evaporation, or the like. The supporting layer 12 may be formed of, for example, a thin metal plate composed of stainless steel (SUS) or the like and having a thickness of, for example, 1.0 mm.

The conducting adhesive 7 is applied to a predetermined position of the electrode pattern 4. The electronic component 6 is mounted on the conductive bonding material 7 and is placed in, for example, an oven set at 120°C to cure the conductive bonding material 7. With respect to a method of applying the conducting adhesive 7, printing using a mesh screen, a metal mask, or the like or dispensing is employed. In this case, the conducting adhesive used as the conductive bonding material 7 is thermosetting and is thus cured with the oven. When a UV curable adhesive is used, curing is performed by UV irradiation. When a cyanoacrylate adhesive is used, curing is performed with a minute

amount of water present on the surface of an adherend. When an anaerobic adhesive is used, curing is performed by blocking air (oxygen).

In step (b), another supporting layer 13 including the electrode pattern 5 provided on a surface thereof is press-bonded onto the component-mounted side of the supporting layer 12 with the prepreg 2 therebetween. At the same time, the prepreg 2 is temporarily cured. By the press-bonding, the electronic component 6 is embedded in the prepreg 2, and the electrode patterns 4 and 5 are bonded to the front and back surfaces of the prepreg 2. As the temporary curing conditions, for example, heat treatment is preferably performed at 120°C for about 10 to 15 minutes. The electrode pattern 5 is formed on the supporting layer 13 by the same process as that for the electrode pattern 4. The material and shape of the supporting layer 13 are identical to those of the supporting layer 12. In this case, an electronic component is not mounted on the surface of the electrode pattern 5 but may be appropriately fixed.

In step (c), after thermocompression-bonding and curing the prepreg 2, the supporting layers 12 and 13 are separated from the temporarily cured prepreg 2, thereby transferring the electrode patterns 4 and 5 onto the front and back surfaces of the prepreg 2. After the separation, the prepreg 2 is completely cured. As the complete curing conditions, for example, heat treatment is preferably performed at 170°C to 200°C for about 1 hour.

In step (d), the through hole or via hole 10 is formed in the

cured resin layer 2 and is then filled with a conducting material to electrically connect the front-side electrode pattern 5 with the back-side electrode pattern 4. The via hole 10 is formed by a laser or drilling. In this way, since the via hole 10 is formed in the cured resin layer 2, the deviation of the connection positions of the via hole 10 and the electrode patterns 4 and 5 caused by curing contraction does not occur, thus resulting in a connection structure with high precision. When the prepreg 2 is cured after separating the supporting layers 12 and 13 from the prepreg 2, it is also possible to form the via hole 10 by irradiating the uncured prepreg with a laser.

In step (e), the electronic component 8 is connected and fixed onto the electrode pattern 5 with the conductive bonding material 9, the electrode pattern 5 being provided on the front side. Also in this case, a conducting adhesive is used as the conductive bonding material 9. The conducting adhesive 9 is preferably cured in an oven set at, for example, 120°C.

In step (f), another supporting layer 14 including the electrode pattern 3 provided on a surface thereof is press-bonded onto the surface of the resin layer 2 with the prepreg 1 therebetween, the surface fixing the electronic component 8. At the same time, the prepreg 1 is temporarily cured. By the press-bonding, the electronic component 8 is embedded in the prepreg 1, and electrode patterns 5 and 3 are bonded onto the front and back surfaces of the prepreg 1. The temporary curing conditions are the same as above. The electrode pattern 3 is preferably formed on the supporting layer 14 by the same process as that for the

electrode pattern 4. The material and shape of the supporting layer 14 are identical to those of the supporting layer 12. In this case, an electronic component is not mounted on the outer layer electrode 3 but may be appropriately connected and fixed using the conductive bonding material.

In step (g), after thermocompression-bonding and curing the prepreg 1, the supporting layer 14 is separated from the temporarily cured prepreg 1, thereby transferring the electrode pattern 3 onto the surface of the prepreg 1. After separation, the prepreg is completely cured. The complete curing conditions are the same as above.

In step (h), the through hole or via hole 11 is formed in the cured resin layer 1 and is then filled with a conducting material to electrically connect the electrode pattern 3 with the electrode pattern 5.

Steps (a) to (h) are included in the process for producing the component-embedded substrate A having two resin layers 1 and 2. By sequentially laminating other resin layers on the outer surface of the resin layer 1 or 2, it is also possible to constitute a component-embedded substrate having a multilayer structure.

As shown in Fig. 2, after connecting the electronic components 6 and 8 with the electrode patterns 4 and 5 using the conductive bonding materials 7 and 9, the prepregs 2 and 1 are press-bonded, thus eliminating the detachment of the electronic components 6 and 8 from the electrode patterns 4 and 5 during the press-bonding of the prepregs 2 and 1, and permitting a reduction in connection resistance. Since the electrode pattern 5 interposed between the

resin layers 1 and 2 is a single layer, the two resin layers 1 and 2 are strongly bonded with the electrode pattern 5 provided therebetween. Therefore, the delamination of the resin layers 1 and 2 from the electrode pattern 5 can be eliminated.

Fig. 3 shows a process for producing a component-embedded substrate B according to the present invention. This process corresponds to the second embodiment.

In step (a), an electrode pattern 21 is formed on a supporting layer 20, and an electronic component 22 is connected and fixed onto the surface of the electrode pattern 21 with a conductive bonding material 23. The supporting layer 20, the electrode pattern 21, and the conductive bonding material 23 are the same as those in the first embodiment shown in Figs. 1 and 2. Thus, the descriptions are omitted.

In step (b), another supporting layer 25 is press-bonded onto the component-mounted surface of the supporting layer 20 with a prepreg 24 therebetween. At the same time, the prepreg 24 is temporarily cured. By press-bonding, the electronic component 22 is embedded in the prepreg 24, and the electrode pattern 21 is bonded to the lower surface of the prepreg 24. The temporary curing conditions are the same as those in the first embodiment.

In step (c), after thermocompression-bonding and curing the prepreg 24, the supporting layers 20 and 25 are separated from the temporarily cured prepreg 24, thereby transferring the electrode pattern 21 to the lower surface of the prepreg 24. Then, the prepreg 24 is completely cured. The complete curing conditions are the same as those in the first embodiment.

In step (d), the cured resin layer 24 is flipped, and an

electronic component 26 is connected and fixed onto the back surface of the electrode pattern 21 with a conductive bonding material 27.

In step (e), another supporting layer 29 is press-bonded onto the surface fixing the electronic component 26 with a prepreg 28 therebetween. At the same time, the prepreg 28 is temporarily cured. By press-bonding, the electronic component 26 is embedded in the prepreg 28, and the prepreg 28 is bonded to the electrode pattern 21. The temporary curing conditions are the same as above.

In step (f), after thermocompression-bonding and curing the prepreg 28, the supporting layer 29 is separated from the temporarily cured prepreg 28. After the separation, the prepreg 28 is completely cured. The complete curing conditions are the same as those in the first embodiment.

As described above, the component-embedded substrate B having a two-layer structure is obtained. Next, electrode patterns are formed on the front and back surfaces of the resin layers 24 and 28, and the inner layer electrode 21 may be connected to the exterior by providing a through hole or a via hole.

As described above, when the electronic components 22 and 26 are connected onto the front and back surfaces of one inner layer electrode 21, the electronic components 22 and 26 are connected and fixed onto the inner layer electrode 21 with the conductive bonding materials 23 and 27, respectively. Thus, the conduction reliability between the inner layer electrode 21 and the electronic components 22 and 26 is high, and the connection resistance can be reduced.

Fig. 4 shows a process for producing a component-embedded substrate C according to the present invention. This process corresponds to the third embodiment.

In step (a), an electrode pattern 31 is formed on a supporting layer 30, and an electronic component 32 is connected and fixed onto the surface of the electrode pattern 31 with a conductive bonding material 33. Since the supporting layer 30, the electrode pattern 31, and the conductive bonding material 33 are identical to those in the first embodiment shown in Figs. 1 and 2, the descriptions are omitted.

In step (b), another supporting layer 35 including an electrode pattern 36 provided on the surface thereof is press-bonded onto the component-mounted surface of the supporting layer 30 with a prepreg 34 therebetween. At the same time, the prepreg 34 is temporarily cured. The temporary curing conditions are the same as those in the first embodiment.

In step (c), after thermocompression-bonding and curing the prepreg 34, the supporting layers 30 and 35 are separated from the temporarily cured prepreg 34. After separation, the prepreg 34 is completely cured. The complete curing conditions are the same as those in the first embodiment.

In step (d), a through hole 37 or a via hole 38 is formed in the cured resin layer 34 and is then filled with a conducting material to electrically connect the front-side electrode pattern 31 with the back-side electrode pattern 36 and to electrically connect the electrode pattern 36 with the external electrode of the electronic component 32. The via hole 37 or 38 is formed by the same process as that in the first embodiment. In this way, since the electrode pattern 36 is electrically connected to the

external electrode of the electronic component 32 through the via hole 38, it is possible to reduce the length of the via hole 38 by the thickness of the electronic component 32 and to reduce the resistance of a conducting path.

In step (e), the cured resin layer 34 is flipped, and an electronic component 39 is connected and fixed onto the back surface of the electrode pattern 31 with a conductive bonding material 40.

In step (f), another supporting layer 42 including an electrode pattern 43 provided on the surface thereof is press-bonded onto the surface fixing the electronic component 39 with a prepreg 41 therebetween. At the same time, the prepreg 41 is temporarily cured. The temporary curing conditions are the same as those in the first embodiment.

In step (g), after thermocompression-bonding and curing the prepreg 41, the supporting layer 42 is separated from the temporarily cured prepreg 41. After the separation, the prepreg 41 is completely cured. The complete curing conditions are the same as those in the first embodiment.

In step (h), a through hole 44 or a via hole 45 is formed in the cured resin layer 41 and is then filled with a conducting material to electrically connect the front-side electrode pattern 43 with the back-side electrode pattern 31 and to electrically connect the electrode pattern 43 with the external electrode of the electronic component 39.

In this component-embedded substrate C, in the same way as for the component-embedded substrate B, the electronic components 32 and 39 are connected and fixed onto the front and back surfaces of

one inner layer electrode 31 with conductive bonding materials 33 and 40. Therefore, the conduction reliability between the inner layer electrode 31 and the electronic components 32 and 39 is high, and the connection resistance can be reduced. Furthermore, the outer layer electrodes 36 and 43 are simultaneously formed by transfer simultaneously with the press-bonding of the prepregs 34 and 41. Thus, the steps of forming the outer layer electrodes 36 and 43 can be omitted.

Fig. 5 shows a process for producing a component-embedded substrate D according to the present invention. This production process provides an exemplary component-embedded substrate including a shield electrode therein.

In step (a), a shield electrode 55 and an electrode pattern 52 that includes an electronic component 53 connected and fixed onto a surface thereof with a conductive bonding material 54 are transferred onto the front and back surfaces of a resin layer 51 to prepare a sheet 50. A process for producing this sheet 50 includes the same steps as, for example, steps (a) to (d) shown in Fig. 2, except that the front-side electrode is the shield electrode 55 covering substantially the entire front surface. The electrode pattern 52 is connected to the shield electrode 55 through the via hole 56.

Another supporting layer 58 including an electrode pattern 59 provided on a surface thereof is press-bonded onto the shield electrode 55 of the sheet 50 with a prepreg 57 therebetween. An electronic component 60 is connected and fixed onto the electrode pattern 59 with a conductive bonding material 61. The prepreg 57 is temporarily cured simultaneously with the press-bonding.

In step (b), the supporting layer 58 is separated. In this state, the prepreg 57 is strongly bonded and fixed onto the back surface of the shield electrode 55. The electronic component 60 is embedded in the prepreg 57. At the same time, the electrode pattern 59 is transferred onto the prepreg 57. Then, the prepreg 57 is completely cured.

In step (c), a via hole 62 is formed in the cured resin layer 57 and is then filled with a conducting material to connect the shield electrode 55 with the electrode pattern 59.

As described above, since the shield electrode 55 functioning as the inner layer electrode is included, noise generated from the electronic component mounted another layer in the component-embedded substrate D and the noise of electromagnetic waves from the exterior can be shielded, and satisfactory electrical characteristics can be obtained. To achieve a satisfactory shielding effect, the electrode area of the shield electrode 55 is required to be at least 60% and preferably at least 90% of the single-layer area (the total of the electrode area and the non-electrode area).

Fig. 6 shows the structure of a component-embedded substrate E according to the present invention.

In this embodiment, in the same way as for the component-embedded substrate D, an example in which a shield electrode is included is provided, except that a shield electrode 70 is provided as the outer layer electrode.

In this component-embedded substrate E, two resin layers 72 and 73 are provided with an inner layer electrode 71 provided therebetween, and electronic components 74 and 75 are connected

and fixed onto the front and back surfaces of the inner layer electrode 71 with conductive bonding materials 76 and 77. The electronic component 74 is a chip component mounted on the inner layer electrode 71 with solder or a conducing adhesive 76. The electronic component 75 is a bare chip mounted on the inner layer electrode 71 with a bump 77. The electrode pattern 71 is connected to a electrode pattern 78 through a via hole 79a. The shield electrode 70 is connected to the inner layer electrode 71 through a via hole 79b.

The component-embedded substrate E is produced by the same process as that shown in Fig. 4, except that the shield electrode 70 is used in place of the electrode pattern 43.

Fig. 7 shows a process for producing a component-embedded substrate F according to the present invention. This process corresponds to the seventh embodiment and provides an exemplary component-embedded substrate having three-layer structure.

Steps (a) to (f) are substantially identical to steps (b) to (h) in the third embodiment (see Fig. 4). Thus, the same reference numerals are assigned, and descriptions are omitted.

In step (g), a component-embedded substrate having a two-layer structure is flipped vertically. In step (h), an electronic component 80 is connected and fixed onto the back surface of the upper-side electrode pattern 36 with a conductive bonding material 81.

In step (i), another supporting layer 83 including an electrode pattern 84 provided on a surface thereof is press-bonded onto the surface fixing the electronic component 80 with a prepreg 82 therebetween. At the same time, the prepreg 82 is temporarily

cured. That is, the prepreg 82 is press-bonded onto the surface of the first layer prepreg 34, the surface being opposite the surface bonded to the second layer prepreg 41.

In step (j), after thermocompression-bonding and curing the prepreg 82, the supporting layer 83 is separated from the temporarily cured prepreg 82.

In step (k), after the temporarily cured prepreg 82 is completely cured, a through hole or via hole 85 is formed in the resin layer 82 and is then filled with a conducting material to electrically connect the front- and back-side electrode patterns 36 and 84. Alternatively, the electrode pattern 84 may be directly connected to the electronic component 80 through the via hole 85.

In this embodiment, the third layer prepreg 82 is laminated on the surface of the first layer prepreg 34, the surface being opposite the surface bonded to the second prepreg 41. The reason for this is described below. After curing the first layer prepreg 34, when the second layer prepreg 41 is laminated and cured, the substrate having the two-layer structure is warped toward the second layer prepreg 41 because of the curing contraction of the second layer prepreg 41. Accordingly, the third layer prepreg 82 is laminated on the surface of the first layer prepreg 34, the surface being opposite the surface bonded to the second layer prepreg 41. Thereby, the substrate that has the two-layer structure and that has been warped toward the second layer prepreg 41 can be warped in the opposite direction because of the curing contraction of the third layer prepreg 82. As a result, it is possible to realize a substrate having a three-layer structure and having a low warpage as a whole.

In the above-described embodiments, the electronic components are connected and fixed onto the electrode patterns with the conducting adhesives. Alternatively, solder may be used, and lead-free solder is preferably used in view of the global environment. For example, Sn containing one to four elements selected from Ag, Bi, Cu, Zn, and In is used.

With respect to the conducting adhesive, a binder that is composed of epoxy or urethane and that contains Ag, Cu, Ni, Au, Sn, Zn, or Pt serving as a conductive material or a mixture of these may be used,

In the above-described embodiments, the prepreg is temporarily cured before separating the supporting layer, and the prepreg is completely cured after separating the supporting layer. Alternatively, the prepreg may be completely cured before separating the supporting layer.

Industrial Applicability

As is clear from the descriptions above, according to the first embodiment of the present invention, a plurality of layers are not laminated in a single step. By sequentially laminating the prepregs and the electrode patterns, it is possible to produce a component-embedded substrate having a multilayer structure. Therefore, the electrode pattern can be connected to the electronic component with the conductive bonding material. The connection resistance between the electrode pattern and the electronic component can be reduced. The connection reliability can be improved.

Furthermore, the inner layer electrode between the prepregs

(resin layers) is a single layer alone and is different from the structure having two inner layer electrodes. Therefore, it is unnecessary to contact and electrically connect the inner layer electrodes to each other. Furthermore, it is possible to prevent the occurrence of delamination between the inner layer electrodes.

The electrode pattern is transferred to the prepreg, and after curing this prepreg, the next prepreg is laminated; hence, the first prepreg is not compressed every lamination, and there is no problem, such as the poor electrical connection of the electrical component embedded in the first prepreg or the deformation of the electrode pattern.

According to the second embodiment, in the case in which the electronic components are connected onto the front and back surfaces of the inner layer electrode, the first electronic component is connected and fixed onto the surface of the first electrode pattern with the conductive bonding material, and the first electrode pattern is transferred to the prepreg. Then, the second electronic component is connected and fixed onto the back surface of the first electrode pattern with the conductive bonding material, and another prepreg is press-bonded onto the back surface of the first electrode pattern. Therefore, it is possible to achieve high conduction reliability between the first electrode pattern serving as the inner layer electrode and the electronic components and to reduce the connection resistance. As a result, it is possible to obtain a component-embedded substrate having reliable electrical characteristics.

According to the third embodiment, in the case in which the electronic components are connected onto the front and back

surfaces of the inner layer electrode, the supporting layer having the electrode pattern is disposed on the surface opposite the press-bonded surface of the prepreg, and then the electrode pattern is transferred simultaneously with press-bonding. Therefore, in addition to an effect obtained in the second embodiment, it is unnecessary to form new electrode pattern after press-bonding the prepreg. Thus, the number of steps can be reduced.